REMARKS

Amendments

Claims 1, 9, and 12 were amended to incorporate the write latch from dependent claims 2, 10, and 16, respectively. Claim 17 was amended to correct a typographical error. Claims 2, 10, and 16 were cancelled without prejudice.

Rejections Under 35 U.S.C. § 103

Claims 1-10, and 12-20 were rejected under 35 U.S.C. § 103 as being unpatentable in view of Hazen et al. (U.S. Patent 6,088,264). Claims 2, 10, and 16 were cancelled hereby without prejudice or disclaimer. Applicant respectfully traverses this rejection and feels that claims 1, 3-9, 12-15, and 17-20, as amended, are allowable for the following reasons.

Applicant respectfully maintains that Hazen et al. teaches a memory which has a separate read/write circuit for each partition. As such, the Applicant submits that Hazen et al. does not disclose or suggest a memory with a read/write circuit that simultaneously supports multiple simultaneous read/write operations, each read/write circuit of Hazen et al. is restricted to executing a single operation at any given time period. *See, e.g.*, Hazen et al., Figure 2, and column 2, line 47 to column 3, line 12. Applicant therefore respectfully submits that Hazen et al. does not teach or suggest a non-volatile memory device with a non-volatile memory array, read/write circuitry coupled to the array, wherein the read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks, and a write latch coupled to the read/write circuitry, wherein the write latch is adapted to store the first data provided on external data communication connections, as maintained by the Examiner.

In addition to the above argument regarding Hazen et al. disclosing a memory device having a memory device with a plurality of read/write circuits, the Applicant further contends that there is no motivation or suggestion to modify the reference in this manner. Specifically, Applicant contends that to modify Hazen et al. to provide writing

to a first bank of a memory array while reading from two or more remaining banks of the memory array would require a modification of Hazen et al.'s user interface and plurality of read/write circuitry to allow the writing to a first bank of a memory array while reading from two or more remaining banks of the memory array with a single read/write circuit. Applicant finds no motivation or suggestion to modify the operation of Hazen et al. expressly or impliedly contained in the Hazen et al. reference, and the Office Action does not provide a convincing line of reasoning as to why an artisan would have found the claimed invention to have been obvious in light of the teachings of the reference. Applicant thus submits that the Office has also failed to meet its burden of establishing a *prima facie* case of obviousness. *See* MPEP § 706.02(j) ("The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.'").

Additionally, the Applicant respectfully maintains that Hazen et al. teaches an asynchronous Flash memory. The Applicant notes that it is well known by those skilled in the art that conventional memory systems are generally divided into asynchronous and synchronous communications. In asynchronous communications the memory controller uses control signals to indicate to the memory when requests for data transactions are sent. The data transfers themselves are also performed asynchronously. These asynchronous communication interactions have difficulty meeting high memory bandwidth demands of many modern computer systems. As a result, synchronous interface standards where the control signals and data transfers are sent at predetermined time periods and in synchronization with a clock signal have been developed. Examples of these synchronous interfaces include, but are not limited to, Synchronous DRAM (SDRAM) and double data rate SDRAM (DDR-SDRAM). Applicant maintains therefore that because Hazen et al. purports to teach an asynchronous Flash memory, it does not

teach or suggest a write latch to aid synchronous timing of data transfers as maintained by the Examiner.

Applicant's claim 1 is directed to a non-volatile memory comprising an array of non-volatile memory cells arranged in a plurality of addressable banks, read/write circuitry coupled to the array, wherein the read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks, and a write latch coupled to the read/write circuitry, wherein the write latch is adapted to store the first data provided on external data communication connections. As detailed above, Applicant submits that Hazen et al. fails to teach or suggest such a memory device. As such, Hazen et al. fails to teach or suggest all elements of independent claim 1.

Applicant's claim 7 is directed to a non-volatile memory comprising an array of non-volatile memory cells arranged in a plurality of addressable banks, a write latch to store first data provided on external data communication connections, and read/write circuitry coupled to the array, wherein the read/write circuitry writes the first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks. As detailed above, Applicant submits that Hazen et al. fails to teach or suggest such a memory device. As such, Hazen et al. fails to teach or suggest all elements of independent claim 7.

Applicant's claim 9 is directed to a processing system comprising a processor, and a non-volatile memory coupled to the processor. The non-volatile memory comprising an array of non-volatile memory cells arranged in a plurality of addressable banks, read/write circuitry coupled to the array, wherein the read/write circuitry writes first data provided by the processor to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks and provides the second data to the processor, and a write latch, wherein the write latch is adapted to store the first data while it is being written to the first one of the plurality of addressable banks. As detailed above, Applicant submits that Hazen et al. fails to teach or suggest such a memory device. As such, Hazen et al. fails to teach or suggest all elements of independent claim 9.

Applicant's claim 12 is directed to a method of operating a non-volatile memory comprising writing first data to a first bank location in a memory array of the non-volatile memory, wherein the first data is stored in a latch circuit prior to writing the first data to the first bank location in the memory array; substantially simultaneously reading second data from a second bank location in the memory array of the non-volatile memory; and substantially simultaneously reading third data from a third bank location in the memory array of the non-volatile memory. As detailed above, Applicant submits that Hazen et al. fails to teach or suggest such a memory device. As such, Hazen et al. fails to teach or suggest all elements of independent claim 12.

Applicant's claim 17 is directed to a method of operating a memory device comprising receiving first externally provided data, storing the first data in a write latch, writing the first data from the write latch to a first bank location in a memory array of the memory device, substantially simultaneously reading second data from a second bank location in the memory array of the memory device, and substantially simultaneously reading third data from a third bank location in the memory array of the memory device. As detailed above, Applicant submits that Hazen et al. fails to teach or suggest such a memory device. As such, Hazen et al. fails to teach or suggest all elements of independent claim 17.

Applicant respectfully contends that the Examiner has not met the burden of establishing a *prima facie* case of obviousness in regards to claims 1, 7, 9, 12, and 17, as amended, and, in addition, that claims 1, 7, 9, 12, and 17 as pending have been shown to be patentably distinct from the cited reference, either alone or in combination with the Examiner's taking of official notice. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1, 7, 9, 12, and 17. As claims 3-6, 8, 13-15, and 18-20 depend from and further define claims 1, 7, 9, 12, and 17, respectively, they are also believed to be allowable.

Claims 1-10, and 12-20 were rejected under 35 U.S.C. § 103 as being unpatentable in view of Nawaki (U.S. Patent 6,081,450). Claims 2, 10, and 16 were cancelled hereby without prejudice or disclaimer. Applicant respectfully traverses this rejection and feels that claims 1, 3-9, 12-15, and 17-20, as amended, are allowable for the following reasons.

Applicant respectfully maintains that Nawaki teaches a non-volatile memory where the word lines of the array can be split through the use of pass gates between memory blocks, where differing memory blocks can be independently accessed through separate word line decoders at opposite ends of the split word lines of the array allowing simultaneous operations to be performed on opposite sides of the split word lines. As such, the Applicant submits that the memory disclosed in Nawaki can only simultaneously execute a single read and write operation at a time. The Applicant therefore respectfully submits that Nawaki does not teach or suggest a non-volatile memory device with a non-volatile memory array, read/write circuitry coupled to the array, wherein the read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks, and a write latch coupled to the read/write circuitry, wherein the write latch is adapted to store the first data provided on external data communication connections, as maintained by the Examiner. *See, e.g.*, Nawaki, Figure 1, Figure 4, column 6, lines 3-13, and column 7, line 59 to column 8, line 4.

The Applicant also disagrees with the Examiner and submits that memory array banks and blocks are well known terms of art in the area of non-volatile memory, and that, as such, one skilled in the art of non-volatile memories would not equate a bank, a large addressable portion of a memory array wherein a row is selected by a word lines and output is taken across a set of columns, with an erase block, an independently eraseable portion of the memory. As stated in the present application, "The synchronous flash memory array architecture is designed to allow sectors to be erased without disturbing the rest of the array. The array is divided into 16 addressable "blocks" that are independently erasable. By erasing blocks rather than the entire array, the total device

endurance is enhanced, as is system flexibility. Only the ERASE and BLOCK PROTECT functions are block oriented. The 16 addressable blocks are equally divided into four banks 104, 106, 108 and 110 of four blocks each. The four banks have simultaneous read-while-write functionality." *See, e.g.*, Application, page 25, lines 24 to 30, and page 6, lines 7-13.

In addition to the above arguments regarding Nawaki disclosing a memory device having a memory array with a plurality of banks and Nawaki teaching or suggesting writing to a first bank of a memory array while reading from two or more remaining banks of the memory array, the Applicant further contends that there is no motivation or suggestion to modify the reference in this manner. Specifically, Applicant contends that to modify Nawaki to provide writing to a first bank of a memory array while reading from two or more remaining banks of the memory array would require a modification of Nawaki's memory array to include banks and interface circuitry to incorporate a write latch and to allow the latching of write data and writing to a first bank of a memory array while reading from two or more remaining banks of the memory array. Applicant finds no motivation or suggestion to modify the operation of Nawaki expressly or impliedly contained in the Nawaki reference, and the Office Action does not provide a convincing line of reasoning as to why an artisan would have found the claimed invention to have been obvious in light of the teachings of the reference. Applicant thus submits that the Office has also failed to meet its burden of establishing a *prima facie* case of obviousness. *See* MPEP § 706.02(j) ("The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.'").

Additionally, the Applicant respectfully maintains that Nawaki teaches an asynchronous Flash memory for read while write operation. The Applicant notes that it is well known by those skilled in the art that conventional memory systems are generally divided into asynchronous and synchronous communications. In asynchronous

communications the memory controller uses control signals to indicate to the memory when requests for data transactions are sent. The data transfers themselves are also performed asynchronously. These asynchronous communication interactions have difficulty meeting high memory bandwidth demands of many modern computer systems. As a result, synchronous interface standards where the control signals and data transfers are sent at predetermined time periods and in synchronization with a clock signal have been developed. Examples of these synchronous interfaces include, but are not limited to, Synchronous DRAM (SDRAM) and double data rate SDRAM (DDR-SDRAM). Applicant maintains therefore that because Nawaki purports to teach an asynchronous Flash memory, it does not teach or suggest a write latch to aid synchronous timing of data transfers as maintained by the Examiner.

Applicant's claim 1 is directed to a non-volatile memory comprising an array of non-volatile memory cells arranged in a plurality of addressable banks, read/write circuitry coupled to the array, wherein the read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks, and a write latch coupled to the read/write circuitry, wherein the write latch is adapted to store the first data provided on external data communication connections. As detailed above, Applicant submits that Nawaki fails to teach or suggest such a memory device. As such, Nawaki fails to teach or suggest all elements of independent claim 1.

Applicant's claim 7 is directed to a non-volatile memory comprising an array of non-volatile memory cells arranged in a plurality of addressable banks, a write latch to store first data provided on external data communication connections, and read/write circuitry coupled to the array, wherein the read/write circuitry writes the first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks. As detailed above, Applicant submits that Nawaki fails to teach or suggest such a memory device. As such, Nawaki fails to teach or suggest all elements of independent claim 7.

Applicant's claim 9 is directed to a processing system comprising a processor, and a non-volatile memory coupled to the processor. The non-volatile memory

comprising an array of non-volatile memory cells arranged in a plurality of addressable banks, read/write circuitry coupled to the array, wherein the read/write circuitry writes first data provided by the processor to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks and provides the second data to the processor, and a write latch, wherein the write latch is adapted to store the first data while it is being written to the first one of the plurality of addressable banks. As detailed above, Applicant submits that Nawaki fails to teach or suggest such a memory device. As such, Nawaki fails to teach or suggest all elements of independent claim 9.

Applicant's claim 12 is directed to a method of operating a non-volatile memory comprising writing first data to a first bank location in a memory array of the non-volatile memory, wherein the first data is stored in a latch circuit prior to writing the first data to the first bank location in the memory array; substantially simultaneously reading second data from a second bank location in the memory array of the non-volatile memory; and substantially simultaneously reading third data from a third bank location in the memory array of the non-volatile memory. As detailed above, Applicant submits that Nawaki fails to teach or suggest such a memory device. As such, Nawaki fails to teach or suggest all elements of independent claim 12.

Applicant's claim 17 is directed to a method of operating a memory device comprising receiving first externally provided data, storing the first data in a write latch, writing the first data from the write latch to a first bank location in a memory array of the memory device, substantially simultaneously reading second data from a second bank location in the memory array of the memory device, and substantially simultaneously reading third data from a third bank location in the memory array of the memory device. As detailed above, Applicant submits that Nawaki fails to teach or suggest such a memory device. As such, Nawaki fails to teach or suggest all elements of independent claim 17.

Applicant respectfully contends that the Examiner has not met the burden of establishing a *prima facie* case of obviousness in regards to claims 1, 7, 9, 12, and 17, and, in addition, that claims 1, 7, 9, 12, and 17 as pending have been shown to be

patentably distinct from the cited reference, either alone or in combination with the Examiner's taking of official notice. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1, 7, 9, 12, and 17. As claims 3-6, 8, 13-15, and 18-20 depend from and further define claims 1, 7, 9, 12, and 17, respectively, they are also believed to be allowable.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims. No new matter has been added and no additional fee is required by this amendment and response.

The Examiner is invited to contact Applicant's representative at the number below if there are any questions regarding this response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

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